

METHOD AND STRUCTURE FOR FORMING STRAINED Si FOR CMOS DEVICES

Abstract

A method for manufacturing a device including an n-type device and a p-type device. In an aspect of the invention, the method involves doping a portion of a semiconductor substrate and forming a gap in the semiconductor substrate by removing at least a portion of the doped portion of the semiconductor substrate. The method further involves growing a strain layer in at least a portion of the gap in the semiconductor substrate. For the n-type device, the strain layer is grown on at least a portion which is substantially directly under a channel of the n-type device. For the p-type device, the strain layer is grown on at least a portion which is substantially directly under a source region or drain region of the p-type device and not substantially under a channel of the p-type device.